ABSTRACT OF THE DISCLOSURE

A method of fabricating an electrically conductive via and an SOI structure and the structure. A substrate and a device wafer are provided and an electrically insulating layer having an outer face is formed on one of the substrate or device wafer. The insulating layer has an electrical interconnect structure therein, a portion extending to the outer face of the insulating structure. The outer surface of the insulating layer is bonded to the other of the substrate or device wafer. A portion of the insulating layer can be disposed between the interconnect structure and at least one of the substrate or device wafer with ultimate interconnection made by applying a voltage across the portion of the insulating layer sufficient to break down the portion of the insulating layer while maintaining the integrity of the remainder of the SOI structure. At least one of the device layer and substrate includes a bond region with the interconnect structure contacting the bond region. A portion of the interconnect structure can be buried within the insulating layer as a separate layer therein. As an alternate embodiment, a planar surface can be formed having areas of the device layer and areas of the insulating layer and that surface can be bonded to a substrate wafer. As a still further embodiment, a layer of electrically insulating material is formed having a surface and an edge is formed extending from the surface through the layer of insulating material. A layer of electrically conductive material is formed on the edge and a patterned etch is provided to selectively remove the conductive material from the edge, leaving the material where the conducting via is desired. Then additional insulating material is deposited and the surface is planarized.